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1 **Turkish entrepreneurs in information and communication industry**
Cetindamar, D.;
Management of Engineering and Technology, 2001. PICMET '01. Portland International Conference on , Volume: Supplement , 29 July-2 Aug. 2001
Pages:100 - 106 vol.2

[Abstract] [PDF Full-Text (632 KB)] **IEEE CNF**

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2 **Semi-adaptive context-tree based lossless image compression**
Ginesta, X.; Kim, S.P.;
Image Processing, 1994. Proceedings. ICIP-94., IEEE International Conference , Volume: 3 , 13-16 Nov. 1994
Pages:881 - 883 vol.3

[Abstract] [PDF Full-Text (244 KB)] **IEEE CNF**

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1 **An environment for the reverse engineering of executable programs**
Cifuentes, C.;
Software Engineering Conference, 1995. Proceedings., 1995 Asia Pacific , 6-9 Dec. 1995
Pages:410 - 419

[Abstract] [PDF Full-Text (792 KB)] **IEEE CNF**

2 **Subspace-based delay estimation for CDMA communication systems**
Bensley, S.E.; Aazhang, B.;
Information Theory, 1994. Proceedings., 1994 IEEE International Symposium on , 27 June-1 July 1994
Pages:138

[Abstract] [PDF Full-Text (60 KB)] **IEEE CNF**

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1 Race checking by context inference

Thomas A. Henzinger, Ranjit Jhala, Rupak Majumdar

June 2004 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2004 conference on Programming language design and implementation**, Volume 39 Issue 6

Full text available: pdf(328.94 KB) Additional Information: full citation, abstract, references, index terms

Software model checking has been successful for *sequential* programs, where predicate abstraction offers suitable models, and counterexample-guided abstraction refinement permits the automatic inference of models. When checking *concurrent* programs, we need to abstract threads as well as the contexts in which they execute. Stateless context models, such as predicates on global variables, prove insufficient for showing the absence of race conditions in many examples. We therefore use ...

Keywords: race conditions, software model checking

2 Performance measurements for multithreaded programs

Minwen Ji, Edward W. Felten, Kai Li

June 1998 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1998 ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems**, Volume 26 Issue 1

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, citings, index terms

Multithreaded programming is an effective way to exploit concurrency, but it is difficult to debug and tune a highly threaded program. This paper describes a performance tool called Tmon for monitoring, analyzing and tuning the performance of multithreaded programs. The performance tool has two novel features: it uses "thread waiting time" as a measure and constructs thread waiting graphs to show thread dependencies and thus performance bottlenecks, and it identifies "semi-busy-waiting" points w ...

3 QPATR and constraint threading

James Kilbury

August 1990 **Proceedings of the 13th conference on Computational linguistics - Volume 3**

Full text available: pdf(330.74 KB) Additional Information: full citation, abstract, references, citings

QPATR is an MS-DOS Arity/PROLOG implementation of the PATR-II formalism for unification grammar. The formalism has been extended to include the constraints of LFG as well as negation and disjunction, which are implemented with the disjunction and negation-as-failure

of PROLOG itself. A technique of *constraint threading* is employed to collect negative and constraining conditions in PROLOG difference lists. The parser of QPATR uses a left-corner algorithm for context-free grammars and inclu ...

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1 Multithreading II: A quantitative framework for automated pre-execution thread selection

Amir Roth, Gurindar S. Sohi

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(2.12 MB) Additional Information: full citation, abstract, references, citings, index terms

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Pre-execution attacks cache misses for which address prediction driven prefetching fails. In pre-execution, copies of cache miss computations are isolated from the main program and launched as separate threads called p-threads whenever the processor anticipates an upcoming miss. P-thread selection is the task of deciding what computations should execute as p-threads and when they should be launched such that total execution time is minimized. It is central to the success of pre-execution.We intr ...

2 Technical papers: concurrency: Assuring and evolving concurrent programs: annotations and policy

Aaron Greenhouse, William L. Scherlis

May 2002 **Proceedings of the 24th international conference on Software engineering**

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings, index terms

Assuring and evolving concurrent programs requires understanding the concurrency-related design decisions used in their implementation. In Java-style shared-memory programs, these decisions include which state is shared, how access to it is regulated, the roles of threads, and the policy that distinguishes desired concurrency from race conditions. These decisions rarely have purely local manifestations in code.In this paper, we use case studies from production Java code to explore the costs and ...

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1 Isolating failure-inducing thread schedules

Jong-Deok Choi, Andreas Zeller

July 2002 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 2002 ACM SIGSOFT international symposium on Software testing and analysis**, Volume 27 Issue 4

Full text available: pdf(488.91 KB) Additional Information: full citation, abstract, references, index terms

Consider a multi-threaded application that occasionally fails due to non-determinism. Using the DEJAVU capture/replay tool, it is possible to record the thread schedule and replay the application in a deterministic way. By systematically narrowing down the difference between a thread schedule that makes the program pass and another schedule that makes the program fail, the Delta Debugging approach can pinpoint the error location automatically---namely, the location(s) where a thread switch cause ...

2 Borrowed-virtual-time (BVT) scheduling: supporting latency-sensitive threads in a general-purpose scheduler

Kenneth J. Duda, David R. Cheriton

April 2000 **ACM SIGOPS Operating Systems Review**, Volume 34 Issue 2

Additional Information: full citation, index terms

3 Borrowed-virtual-time (BVT) scheduling: supporting latency-sensitive threads in a general-purpose scheduler

Kenneth J. Duda, David R. Cheriton

December 1999 **ACM SIGOPS Operating Systems Review , Proceedings of the seventeenth ACM symposium on Operating systems principles**, Volume 33 Issue 5

Full text available: pdf(1.81 MB) Additional Information: full citation, abstract, references, citings, index terms

Systems need to run a larger and more diverse set of applications, from real-time to interactive to batch, on uniprocessor and multiprocessor platforms. However, most schedulers either do not address latency requirements or are specialized to complex real-time paradigms, limiting their applicability to general-purpose systems.In this paper, we present *Borrowed-Virtual-Time (BVT) Scheduling,* showing that it provides low-latency for real-time and interactive applications yet weighted sharin ...

4 Thread scheduling for out-of-core applications with memory server on multicomputers
Yuanyuan Zhou, Limin Wang, Douglas W. Clark, Kai Li
May 1999 **Proceedings of the sixth workshop on I/O in parallel and distributed systems**
Full text available: pdf(861.70 KB) Additional Information: full citation, references, index terms

5 Scheduling threads for low space requirement and good locality
Girija J. Narlikar
June 1999 **Proceedings of the eleventh annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.69 MB) Additional Information: full citation, references, citings, index terms

6 Kernel-level scheduling for the nano-threads programming model
Eleftherios D. Polychronopoulos, Xavier Martorell, Dimitrios S. Nikolopoulos, Jesus Labarta, Theodore S. Papatheodorou, Nacho Navarro
July 1998 **Proceedings of the 12th international conference on Supercomputing**
Full text available: pdf(1.20 MB) Additional Information: full citation, references, citings, index terms

7 How "hard" is thread partitioning and how "bad" is a list scheduling based partitioning algorithm?
Xinan Tang, Guang R. Gao
June 1998 **Proceedings of the tenth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.27 MB) Additional Information: full citation, references, citings, index terms

8 Thread scheduling for multiprogrammed multiprocessors
Nimar S. Arora, Robert D. Blumofe, C. Greg Plaxton
June 1998 **Proceedings of the tenth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.77 MB) Additional Information: full citation, references, citings, index terms

9 Thread partitioning and scheduling based on cost model
Xinan Tang, J. Wang, Kevin B. Theobald, Guang R. Gao
June 1997 **Proceedings of the ninth annual ACM symposium on Parallel algorithms and architectures**
Full text available: pdf(1.49 MB) Additional Information: full citation, references, citings, index terms

10 Thread scheduling for cache locality
James Philbin, Jan Edler, Otto J. Anshus, Craig C. Douglas, Kai Li
October 1996 **Proceedings of the seventh international conference on Architectural support for programming languages and operating systems**, Volume 30 , 31 Issue 5 , 9
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a method to improve the cache locality of sequential programs by scheduling fine-grained threads. The algorithm relies upon hints provided at the time of thread creation to determine a thread execution order likely to reduce cache misses. This technique may be particularly valuable when compiler-directed tiling is not feasible. Experiments with several application programs, on two systems with different cache structures, show that our thread scheduling method can improve pro ...

11 Hardware Scheduling for Dynamic Adaptability using External Profiling and Hardware Threading

Brian Swahn, Soha Hassoun

November 2003 **Proceedings of the 2003 International Conference on Computer-Aided Design (ICCAD'03) - Volume 00**

Full text available: Publisher Site Additional Information: full citation, abstract

While performance, area, and power constraints have been thedriving force in designing current communication-enabled embeddedsystems, post-fabrication and run-time adaptability is now required.Two dominant configurable hardware platforms are processorsand FPGAs. However, for compute-intensive applications,neither platform delivers the needed performance at the desiredlow power. The need thus arises for custom, application-specificconfigurable (ASC) hardware.This paper addresses the optimization ...

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